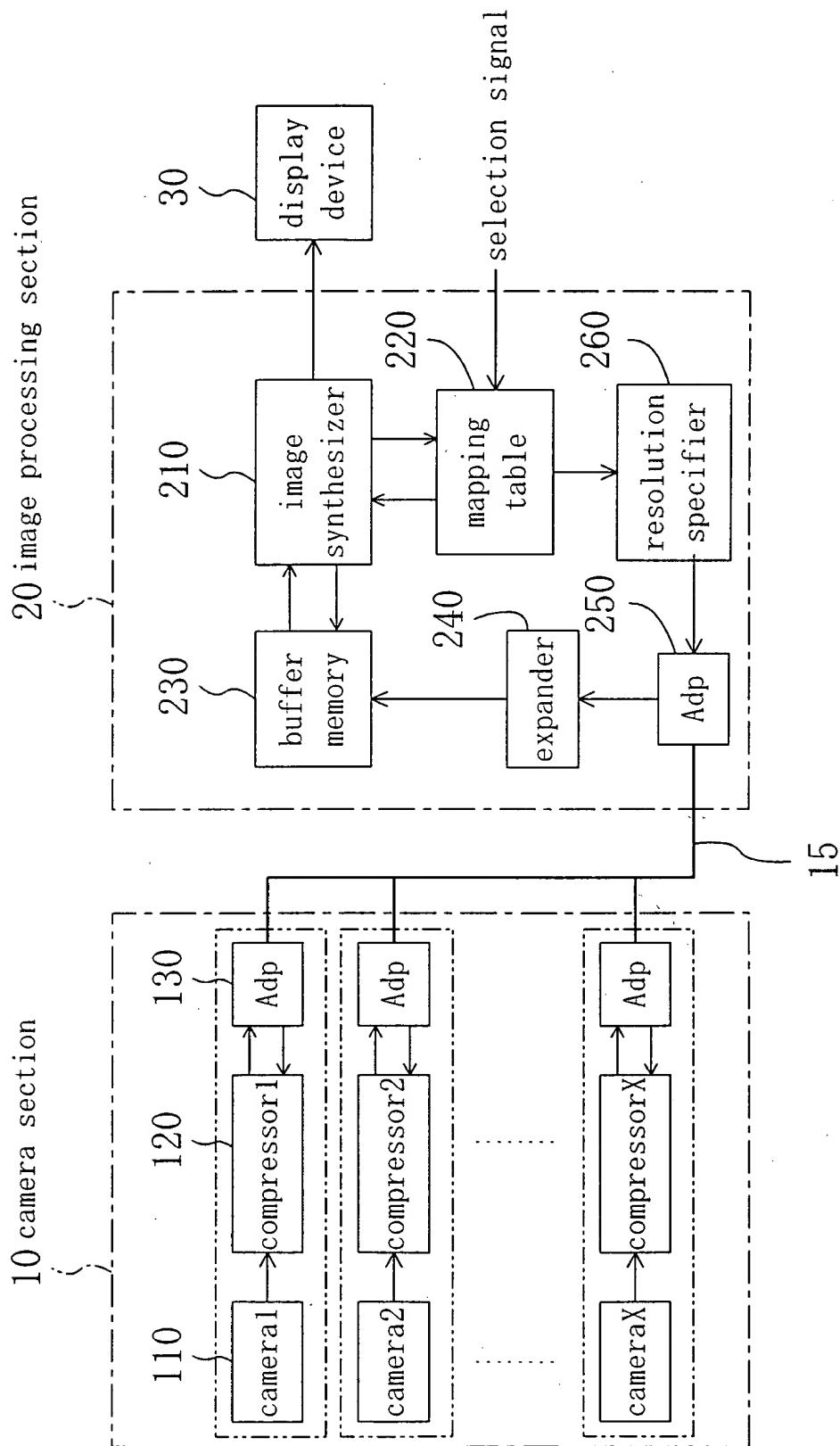


FIG. 1



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FIG. 2

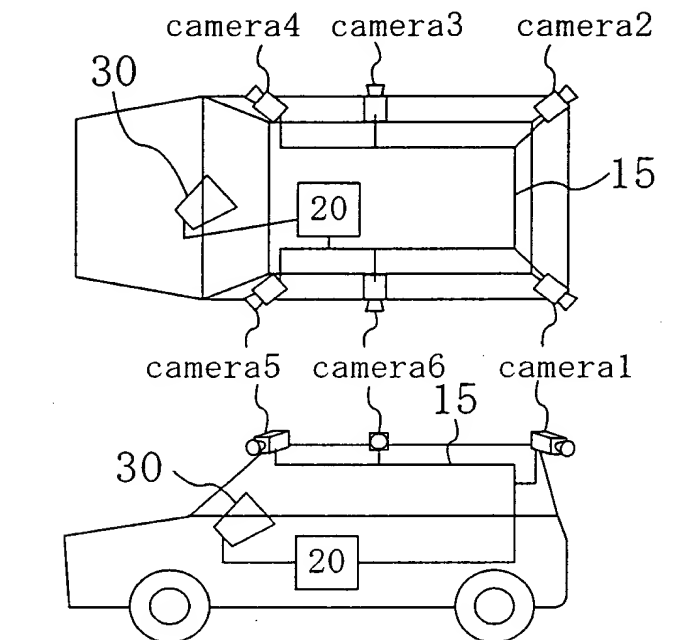


FIG. 2

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FIG. 3

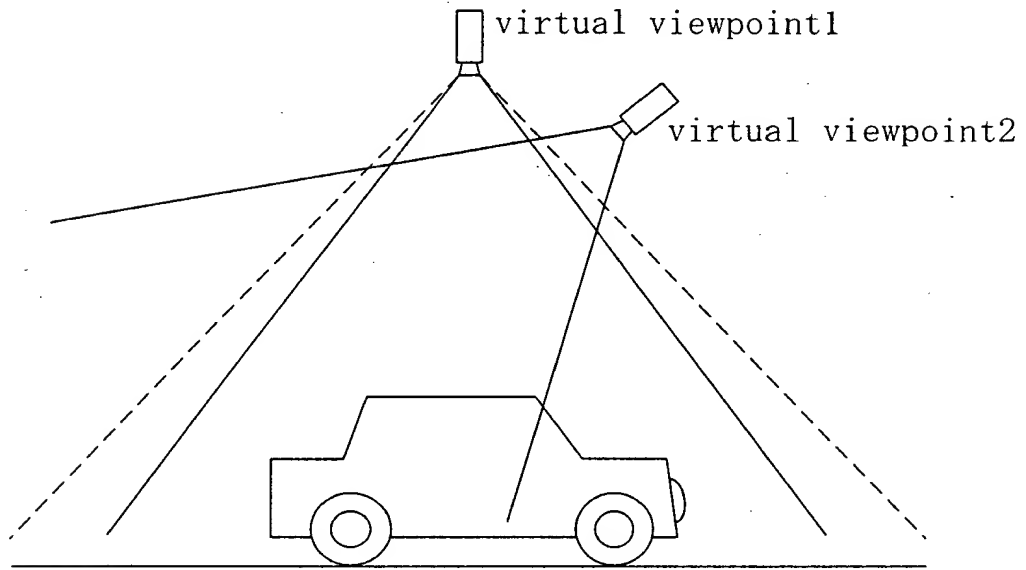


FIG. 3

FIG. 4A

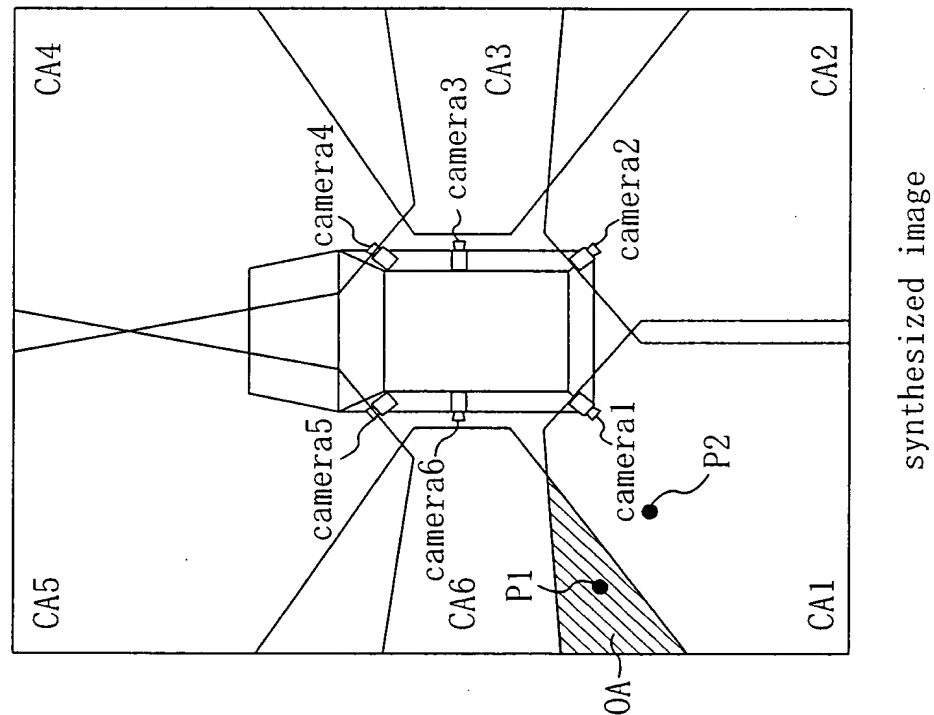


FIG. 4B

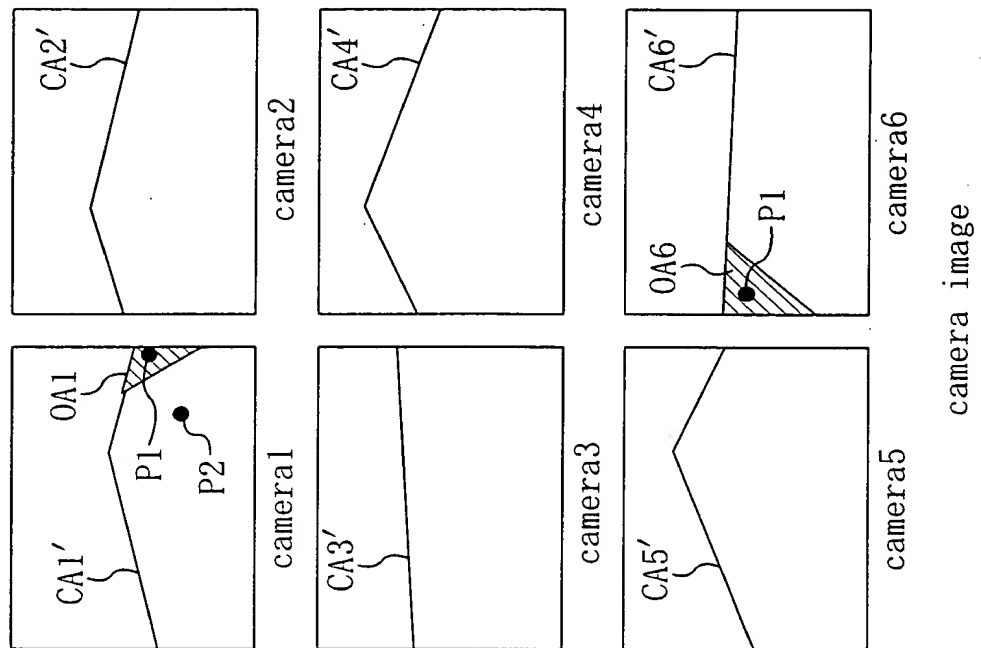


FIG. 5A

<synthesized image>

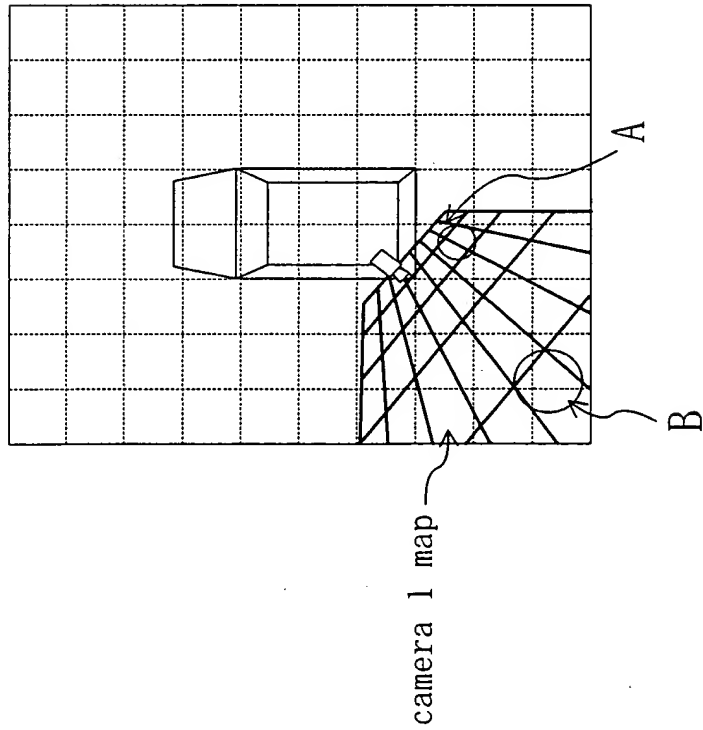


FIG. 5B

<camera 1>

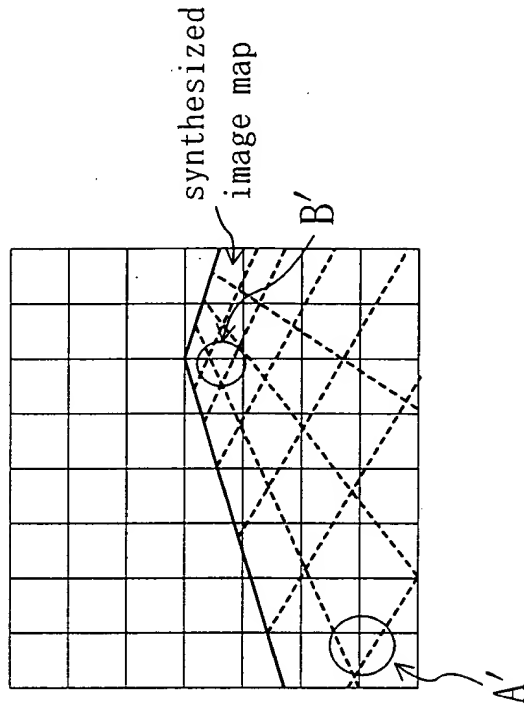


FIG. 6A

<camera 1>

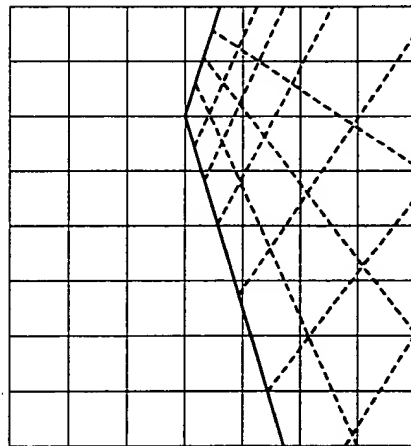
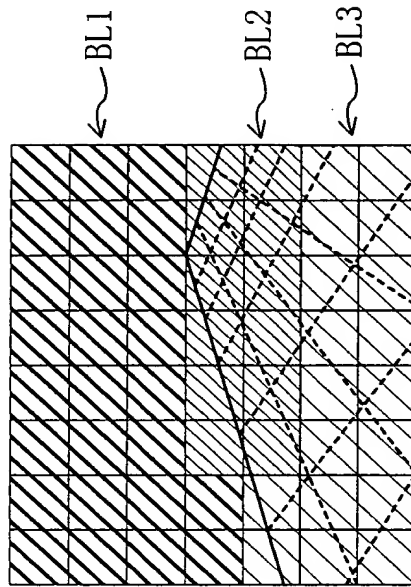


FIG. 6B

<necessary resolutions>



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FIG. 7A

<synthesized image>

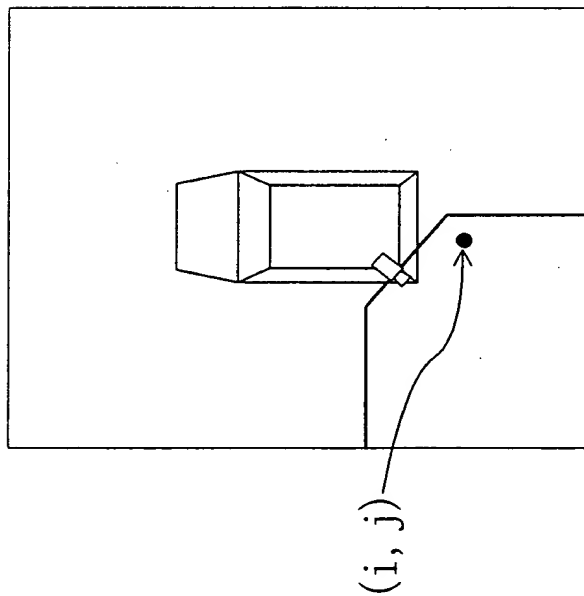


FIG. 7B

<camera 1>

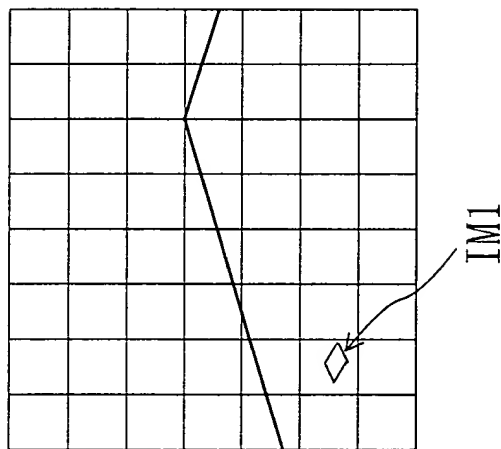


FIG. 7C

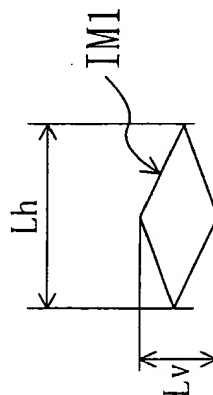
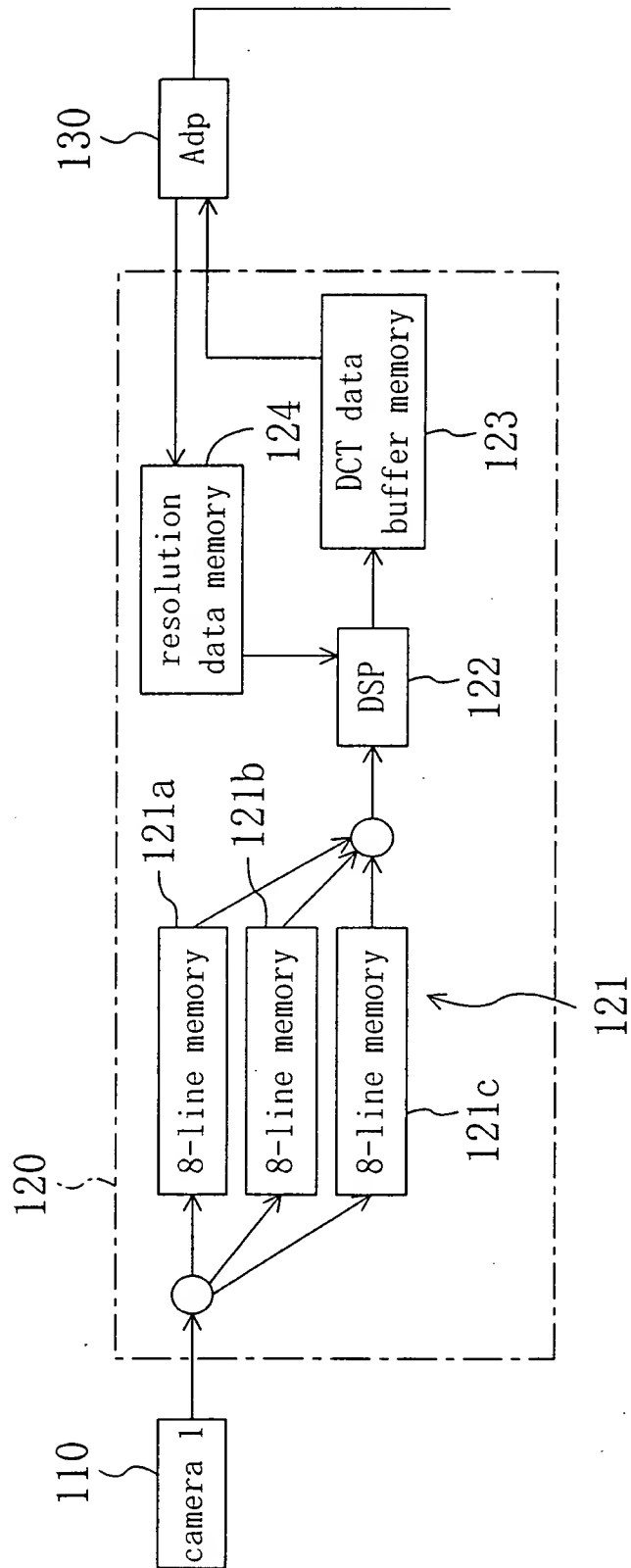


FIG. 7A

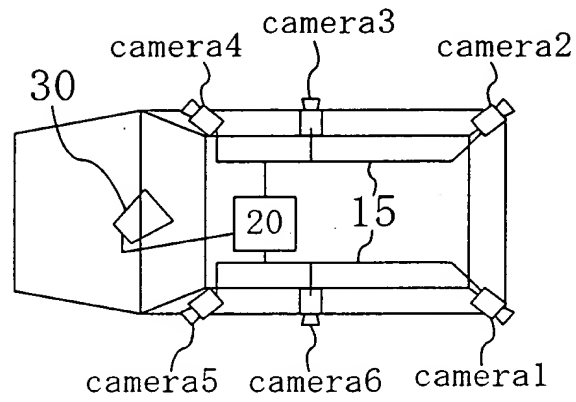
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FIG. 8



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FIG. 9



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FIG. 10

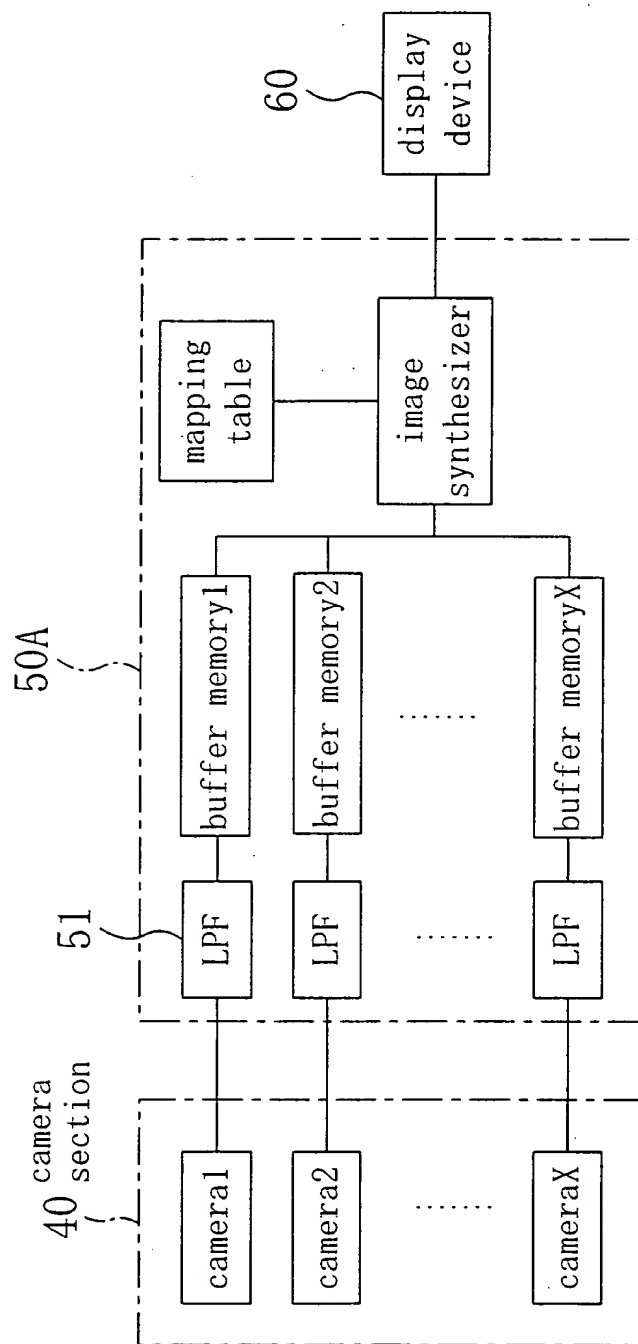


FIG. 10

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FIG. 11A

<camera 1>

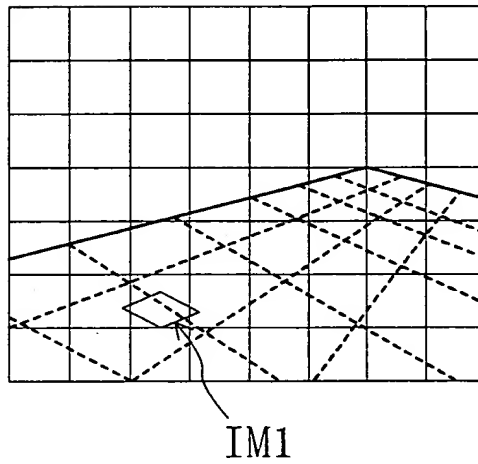
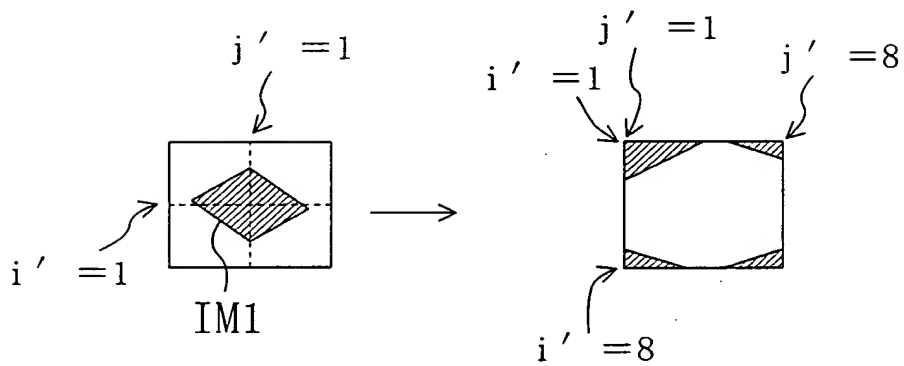


FIG. 11B



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FIG. 12

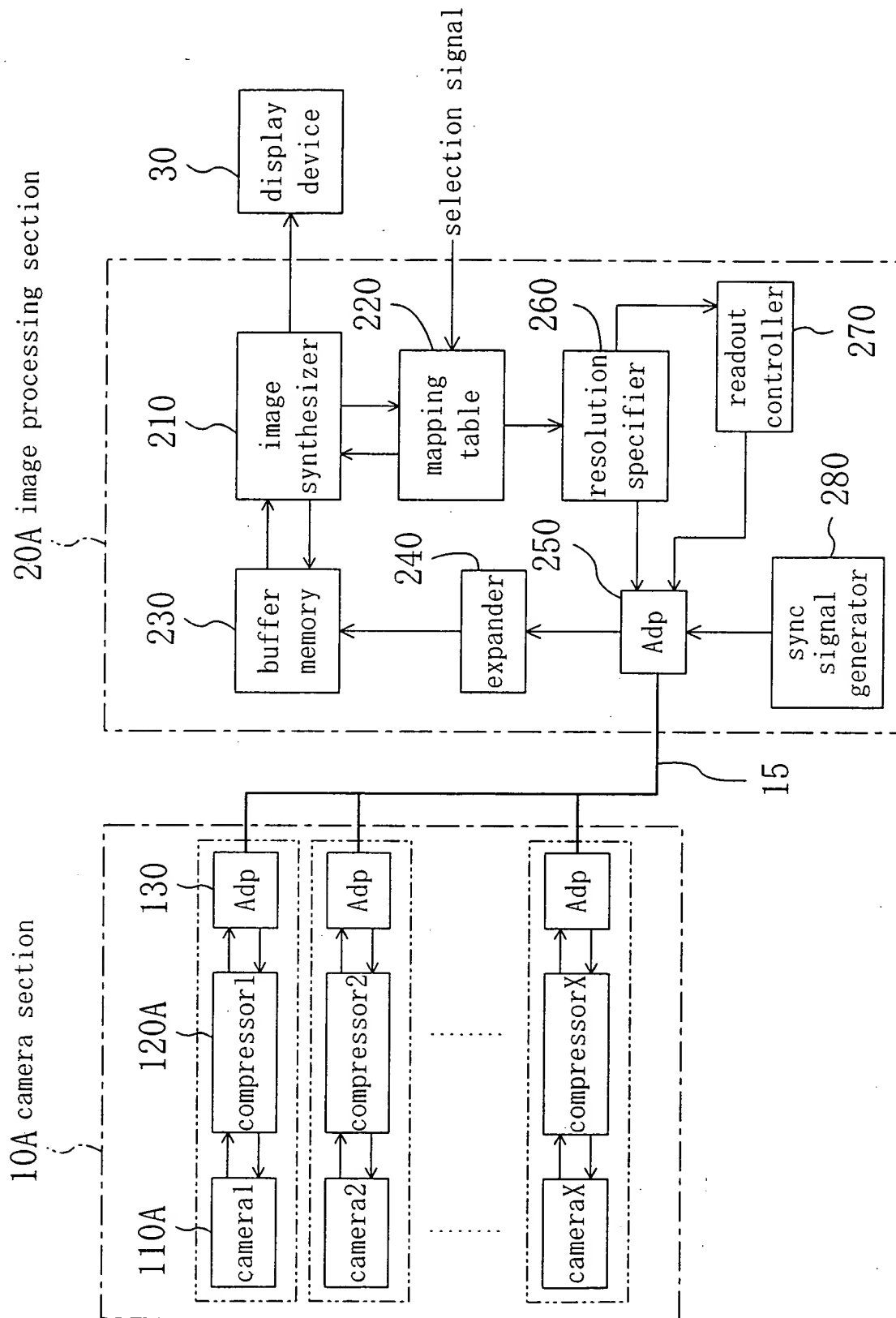
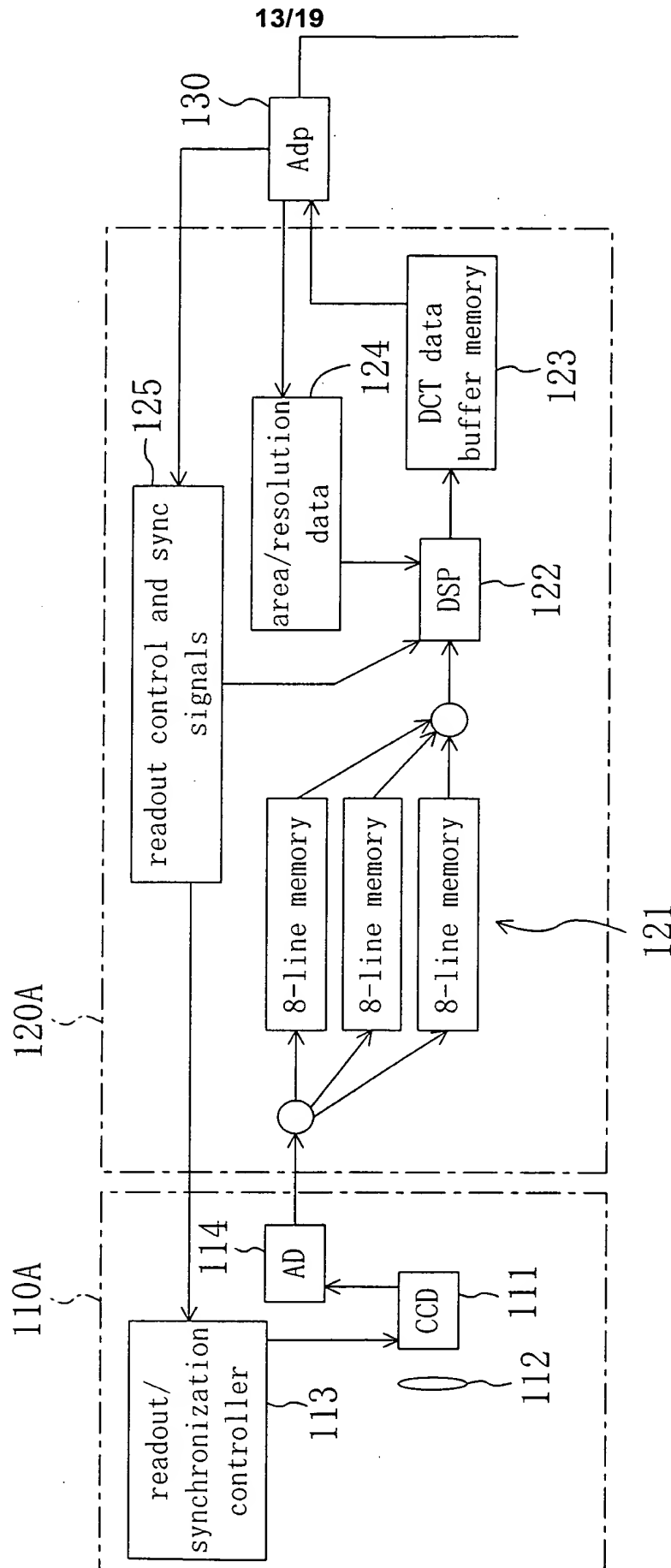


FIG. 12

FIG. 13



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FIG. 14

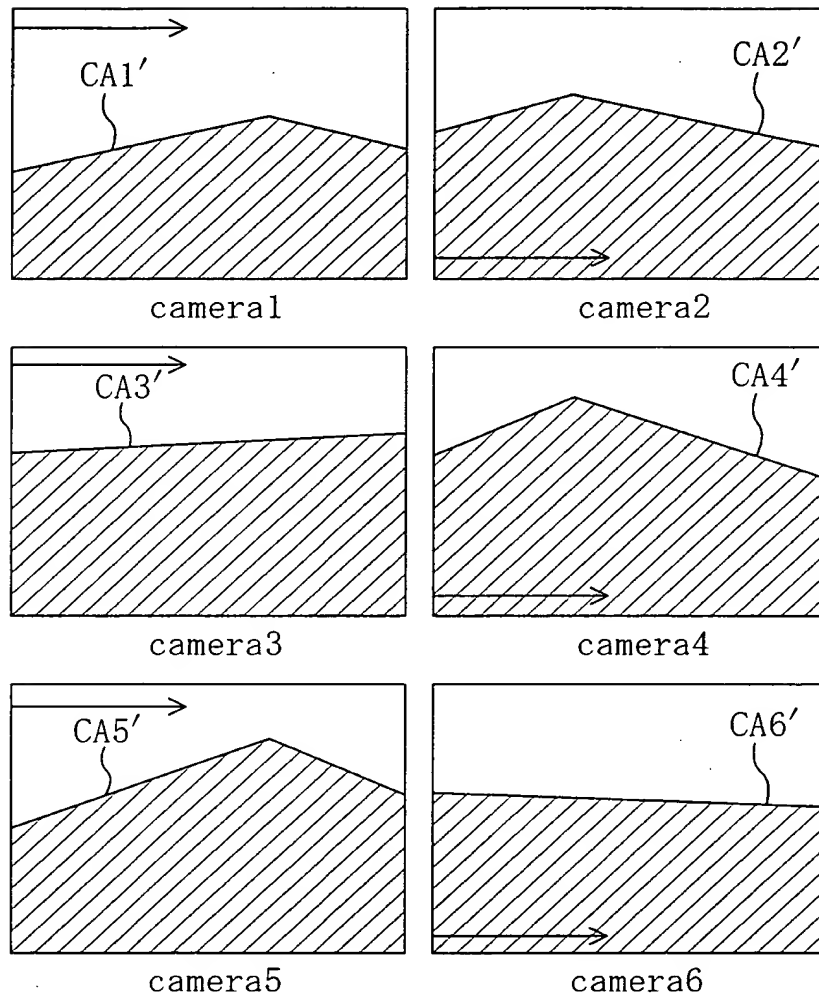


FIG. 14

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FIG. 15

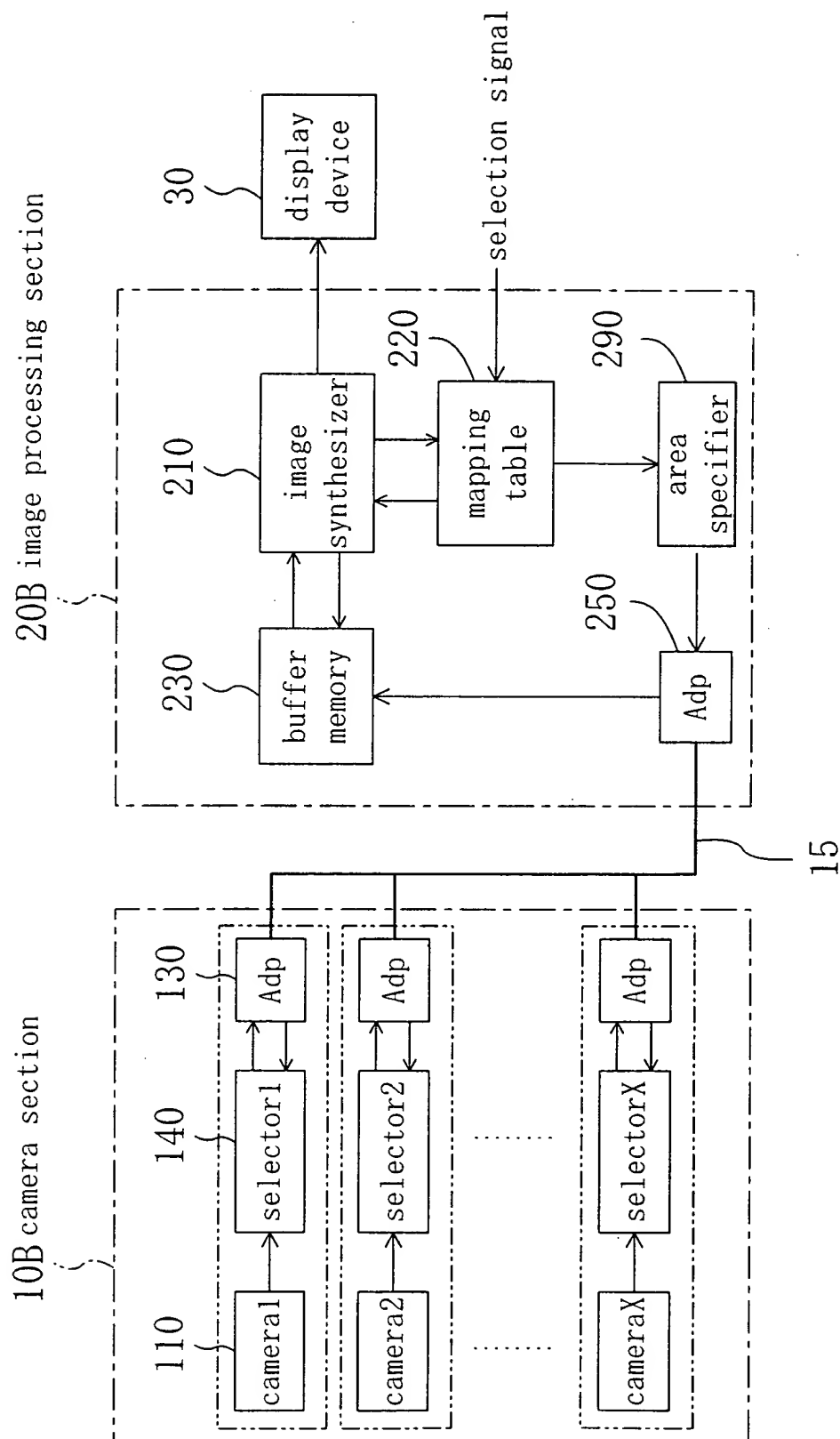


FIG. 15

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FIG. 16B

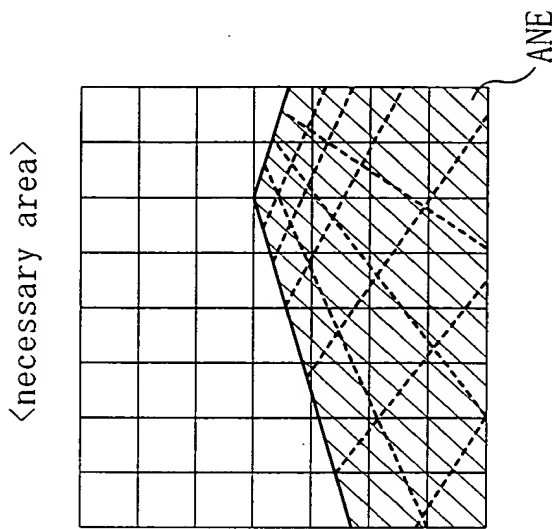


FIG. 16A

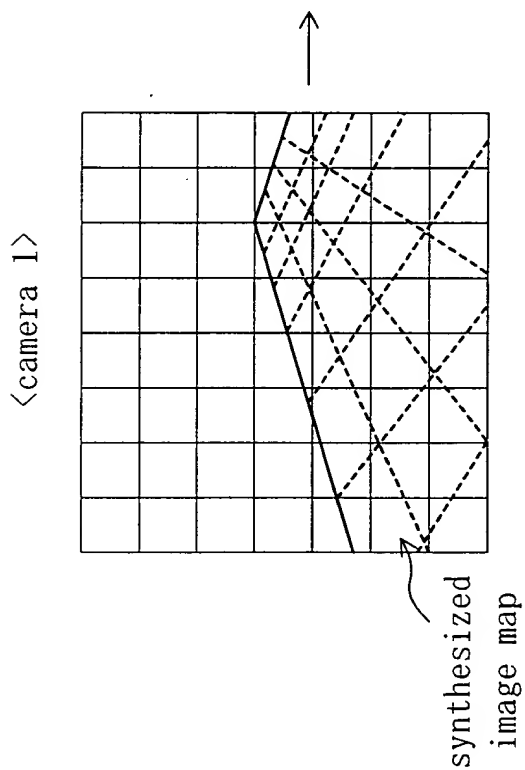


FIG. 17B

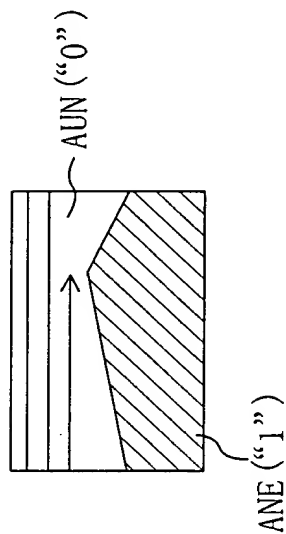
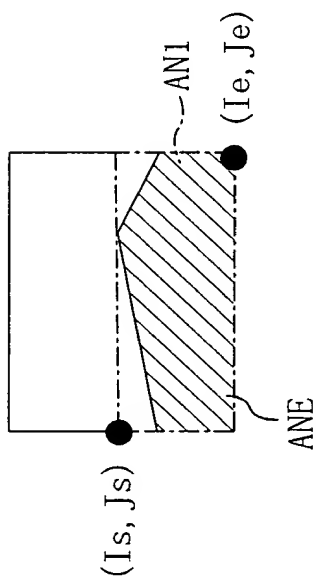


FIG. 17A



The diagram illustrates a video processing system 100. It consists of a camera 110, a video processing unit 140, and an AD converter 130. The video processing unit 140 is enclosed in a dashed box and contains three parallel line memory blocks (141a, 141b, 141c), a summing junction, a DSP 142, an area data memory 144, and a data buffer memory 143. Data flows from the camera 110 through the line memories and summing junction to the DSP 142, then to the area data memory 144, and finally to the AD converter 130. The AD converter 130 also outputs data back to the area data memory 144.

FIG. 19
PRIOR ART

